SUB C1

28. (Amended) A semiconductor integrated circuit comprising:

an HVMISFET (high withstand voltage MOSFET) having:

a source region and drain region of a second conductivity type formed apart from each other on a surface of a semiconductor region of a first conductivity type,

a channel-forming region which is the surface of the semiconductor region between the source region and the drain region,

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a gate formed on the channel-forming region via a gate insulating film of a thickness in the range of 100 – 200 Å,

the drain region being constituted of a low concentration drain region and a high-concentration drain region in contact with each other,

the low-concentration drain region being disposed between the channel-forming region and the high concentration drain region, and

a field insulating film with a thickness at least one order of ten greater than that of the gate insulating film formed by self-alignment above the low-concentration drain region; and

an LVMISFET (low withstand voltage MOSFET) of the same conductivity type formed on the same semiconductor region and having the same threshold voltage and gate insulating film as the HVMISFET,

a surface concentration of the semiconductor region directly under the gate insulating film being partially increased to make the threshold voltage not less than 0.7 V and

drain regions and source regions of the HVMISFET and the LVMISFET being constituted as phosphorus impurity regions.